PVP 12

Code: EC6T1

III B.Tech - II Semester – Regular Examinations - April 2016

VLSI DESIGN

(ELECTRONICS & COMMUNICATION ENGINEERING)

Duration: 3 hours Max. Marks: 70

Answer any FIVE questions. All questions carry equal marks

1. a) Explain the steps involved in PMOS fabrication process. 7 M

   b) Compare CMOS & Bipolar Technologies. 7 M

2. a) Show that the pull-up to pull-down ratio for a NMOS inverter driving another NMOS inverter through one or more pass transistors is 8:1. 7 M

   b) Derive the expression for drain-to-source current for a NMOS enhancement mode transistor. 7 M

3. a) Give the CMOS Stick diagram encodings and explain. 7 M

   b) Draw the layout diagram for a NMOS 3-Input NAND gate. 7 M

4. a) How the propagation delay increases in pass transistor technology. Explain with the help of neat diagram and mathematical expressions. 7 M

b) Explain the following. 7 M

i) Sheet resistance ii) Area Capacitance

5. a) Mention the list of scaling models. Derive the simple Expressions for various key parameters. 7 M

b) Explain the limits on logic levels and power supplies due to noise in detail. 7 M

6. a) Explain the architecture details of Gate Arrays and Standard Cells. 7 M

b) Implement a Full Adder circuit using Programmable Logic Array. 7 M

7. a) Write the features of Xilinx 3000 series FPGAs. 7 M

b) Draw and explain the Input/ Output Block of Xilinx 4000 series FPGA. 7 M

8. a) Explain the role and importance of testing in VLSI. 7 M

b) Explain the following. 7 M

i) Built-In-Self-Test ii) Boundary Scan